Remarks/Arguments:

Applicant appreciatively acknowledges the Examiner's confirmation of receipt of applicant's claim for priority under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application is requested.

Claims 1 to 16 remain in the application.

In item 7 on page 3 of the above-identified Office action, claims 1 t o 16 have been rejected as being fully anticipated by Nunziata under 35 U.S.C. § 102.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method for operating an integrated memory unit having a memory cell field, including the steps of:

before a memory access, partitioning the memory cell field into a plurality of memory areas;

for a memory access, selecting one of the memory areas by applying a memory area address;

during the memory access, internally generating addresses with the memory unit for the access to memory cells of one of the memory areas; and

transmitting the memory area address, and, subsequently and successively, transmitting access data of the one of the memory areas through a common external terminal connection of the memory unit.

United States Patent No. 5,619,471 to Nunziata describes a memory system and a method for controlling DRAM. End users can populate the Nunziata memory system, including banks of memory, with any of a variety of DRAM chips. A memory controller 20 sizes each memory bank. When two banks are both populated to provide the same memory capacity, then the memory controller 20 will operate on those two banks in an interleaved manner. When the paired banks are not populated with the same size DRAM chips, then the memory controller 20 will operate upon each populated bank in a non-interleaved

manner. The Nunziata memory controller 20 includes a bank selection logic configured to account for both size and interleaved or non-interleaved status when determining which memory bank contains a memory location of interest. Row and column addressing is selected to minimize decoding of an incoming system address and to reduce DRAM access time.

In contrast to Nunziata, the invention of the instant application discloses a method for operating an integrated memory unit that enables a memory access for reading or writing data with a comparatively low number of terminal pins. Nunziata does not even suggest this feature.

In a first step set forth in claim 1, before the memory access, the memory cell field is partitioned into a plurality of memory areas. The number of memory areas to be defined is communicated to the memory unit. See page 11, lines 6 to 7, of the specification of the instant application.

The next step is referred to as multiplexing of an address and is associated with a very large number of subsequent access data at one pin. For the memory access, one of the memory areas is selected by applying a memory area address. The memory area address and, subsequently, one after the other, access data of the relevant memory areas, are transmitted

through at least one common external terminal connection of the memory unit. See, e.g., page 2, line 20, through page 3, line 21, of the specification of the instant application.

In contrast to the invention of the instant application, Nunziata does not disclose or suggest a "**common** external terminal connection of the memory unit" for transmitting address and data signals to the DRAM (see claim 1), but, instead, provides a transmission of address and data signals to the DRAM to separate terminal connections by different bus systems. The Nunziata system bus 16 includes an address bus, a data bus, **and** a control bus. The addresses are transmitted to the memory controller 20. See Nunziata at col. 4, lines 1 to 11. The memory controller 20 sends address and control signals to the DRAM 30. Id. Therefore, address and control signal lines are connected between the memory controller 20 and each of the banks of the DRAM 30, which is shown, in particular, in Nunziata at FIG. 2 and is described in col. 5, lines 12 through 16, therein. For a read access, the Nunziata DRAM responds by placing data on the system bus 16. For a write access, data signals are written from the system bus 16 into locations in DRAM 30. See, e.g., Nunziata at col. 3, line 61, through column 4, line 6.

Because Nunziata does not disclose or suggest the claim method

for operating an integrated memory with a low number of necessary terminal pins, Nunziata cannot be said to anticipate the invention of claim 1. Simply put, Nunziata does not disclose or suggest the feature of a **common** external terminal connection for transmitting address and data signals.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

Insofar as claim 1 is allowable, and due to the fact that claim 16 is ultimately depend upon claim 1, the rejection of this claim in item 9 on pages 6 to 7 of the above-identified Office action is now believed to be moot.

In view of the foregoing, reconsideration and allowance of claims 1 to 16 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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